HARRIS Semiconductor

IRF510, IRF511, IRF512, IRF513

4.9A, and 5.6A, 80V and 100V, 0.54 and 0.74 Ohm, N-Channel Power MOSFETs

January 1998

Features

- **4.9A, and 5.6A, 80V and 100V**
- **$r_{DS(ON)}$ = 0.54Ω and 0.74Ω**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF510	TO-220AB	IRF510
IRF511	TO-220AB	IRF511
IRF512	TO-220AB	IRF512
IRF513	TO-220AB	IRF513

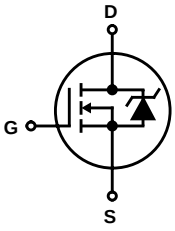
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

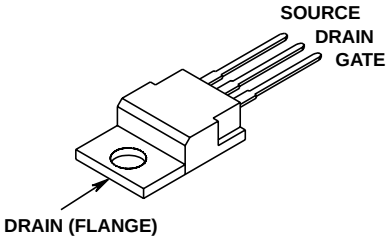
Formerly developmental type TA17441.

Symbol



Packaging

JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1573.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRF510	IRF511	IRF512	IRF513	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DS}	100	80	100	80	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1). . . . . V_{DGR}	100	80	100	80	V
Continuous Drain Current . . . . . I_D	5.6	5.6	4.9	4.9	A
$T_C = 100^oC$ . . . . . I_D	4	4	3.4	3.4	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	20	20	18	18	A
Gate to Source Voltage. . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation. . . . . P_D	43	43	43	43	W
Linear Derating Factor	0.29	0.29	0.29	0.29	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4) . . . . . E_{AS}	19	19	19	19	mJ
Operating and Storage Temperature Range. . . . . T_J, T_{STG}	-55 to 175	-55 to 175	-55 to 175	-55 to 175	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from 25ase for 10s . . . . . T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

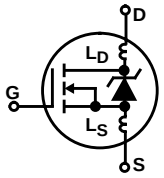
NOTE:

1. $T_J = 25^oC$ to 150^oC.

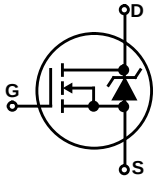
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA, (Figure 10)				
IRF510 IRF512			100	-	-	V
IRF511, IRF513			80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA	2.0	-	4.0	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V $T_J = 150^oC$	-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V, (Figure 7)				
IRF510, IRF511			5.6	-	-	A
IRF512, IRF513			4.9	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.4A, (Figures 8, 9)				
IRF510, IRF511			-	0.4	0.54	Ω
IRF512, IRF513			-	0.5	0.74	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{GS} = 50V, I_D = 3.4A, (Figure 12)	1.3	2.0	-	S
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 5.6A, R_{GS} = 24Ω , V_{DD} = 50V, R_L = 9Ω	-	8	11	ns
Rise Time	t_r	V_{DD} = 50V, V_{GS} = 10V, (Figures 17, 18) MOSFET switching times are essentially independent of operating temperature	-	25	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	15	21	ns
Fall Time	t_f		-	12	21	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA (Figures 14, 19, 20) Gate charge is essentially independent of operating temperature	-	5.0	7.7	nC
Gate to Source Charge	Q_{gs}		-	2.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	3.0	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz, (Figure 11)		-	135	-	pF
Output Capacitance	C_{OSS}			-	80	-	pF
Reverse-Transfer Capacitance	C_{RSS}			-	20	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw On Tab To Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.5	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free air operation		-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	Test Conditions		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	5.6	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	20	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 5.6A, V_{GS} = 0V (Figure 13)		-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 5.6A, dI_{SD}/d_t = 100A/µs		4.6	96	200	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, I_{SD} = 5.6A, dI_{SD}/d_t = 100A/µs		0.17	0.4	0.83	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 25V, start $T_J = 25^oC$, L = 910µH, R_G = 25Ω, peak I_{AS} = 5.6A (See Figure 15, 16).

Typical Performance Curves Unless Otherwise Specified

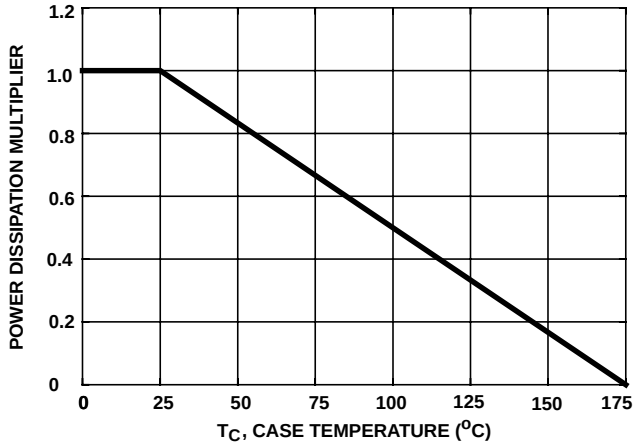


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

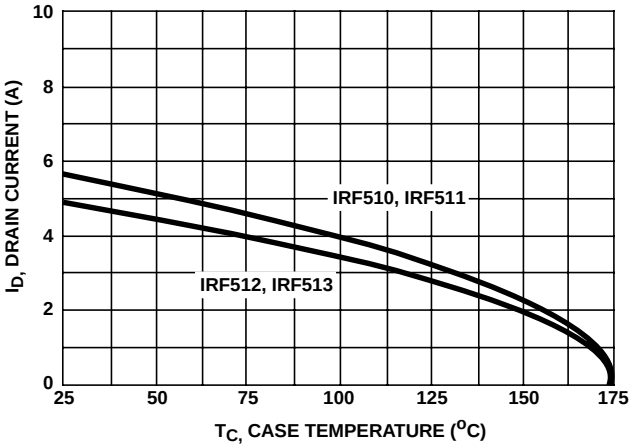


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

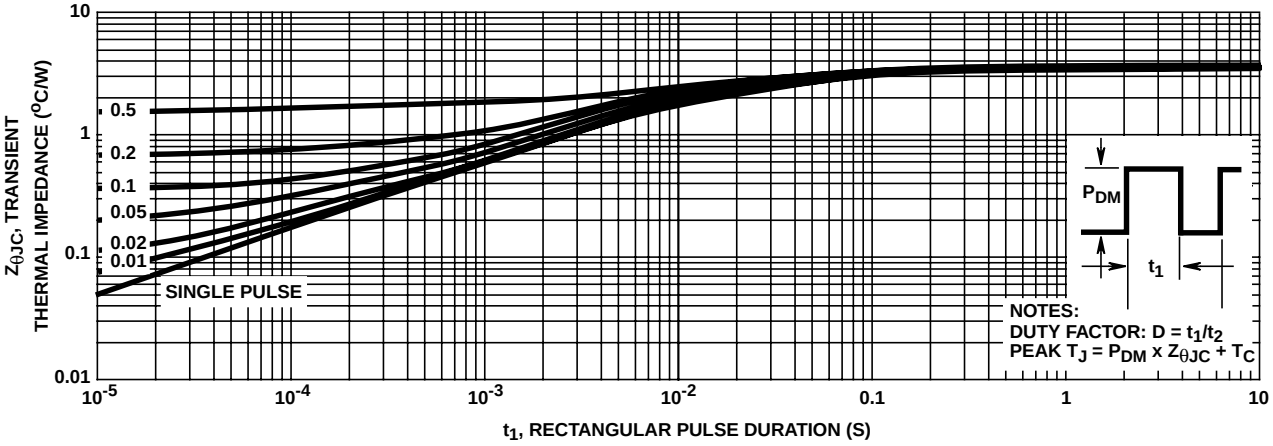


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

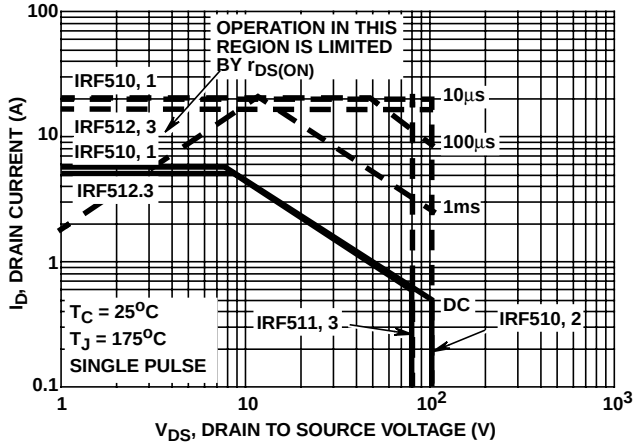


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

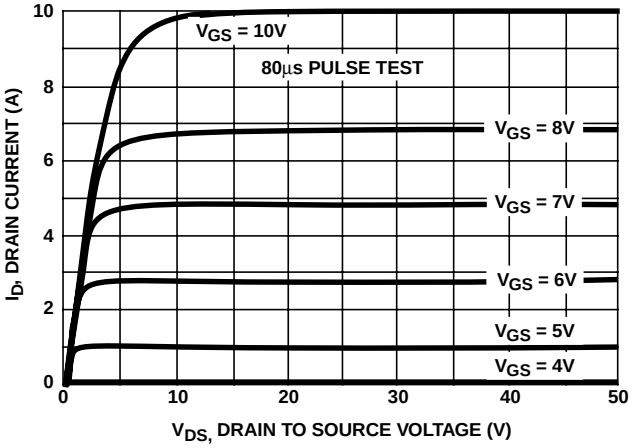


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

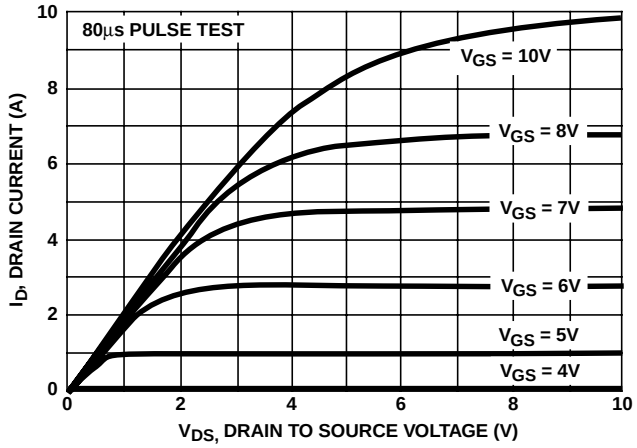


FIGURE 6. SATURATION CHARACTERISTICS

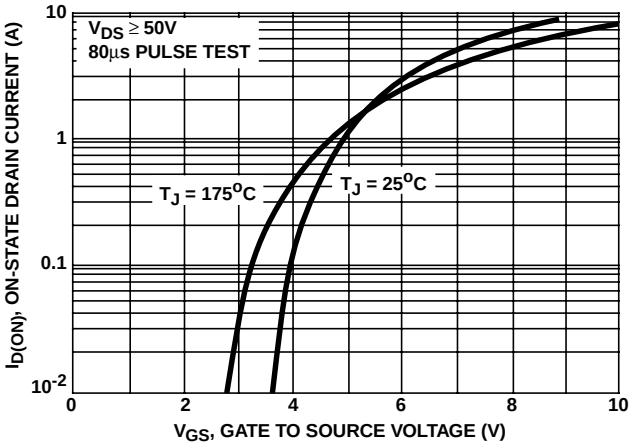


FIGURE 7. TRANSFER CHARACTERISTICS

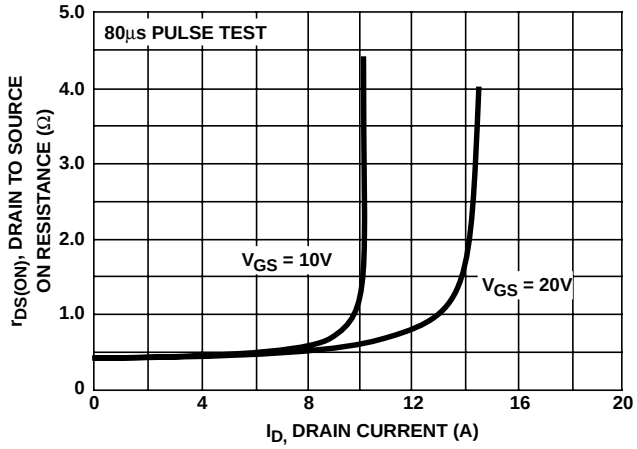


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

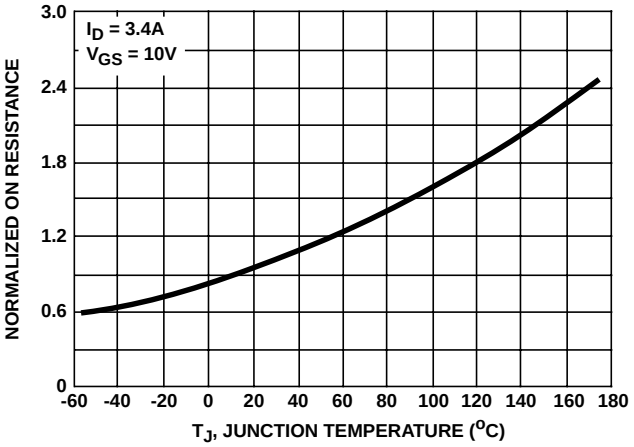


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

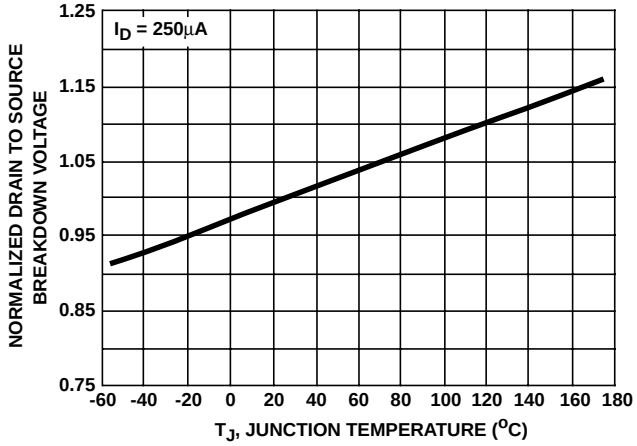


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

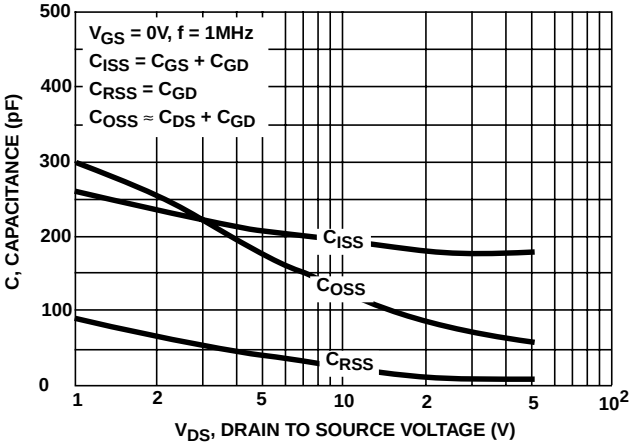


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

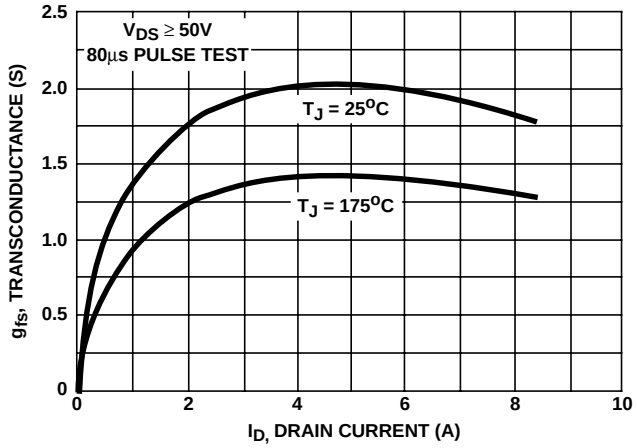


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

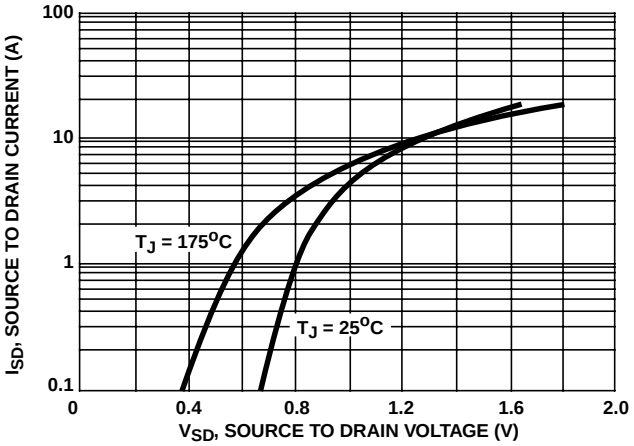


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

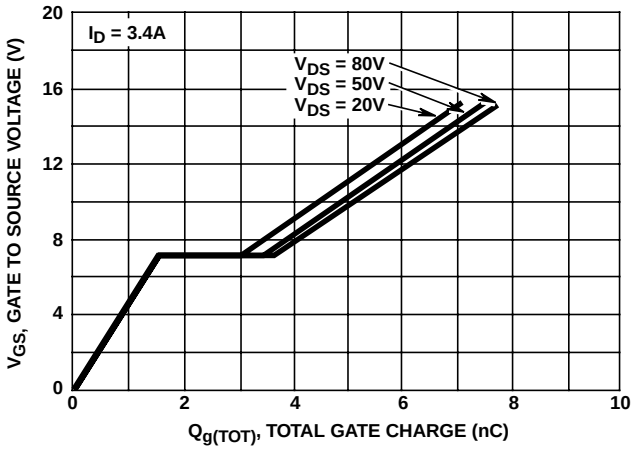


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

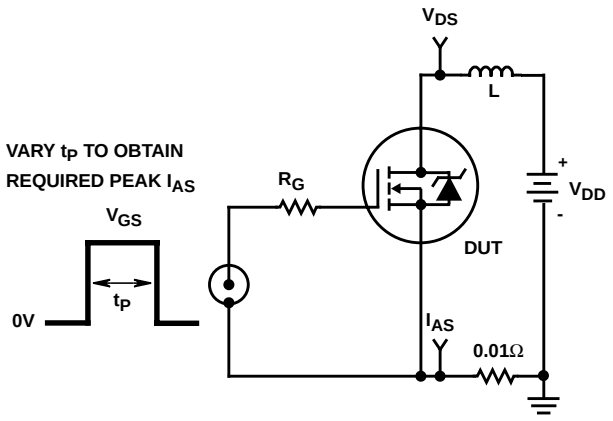


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

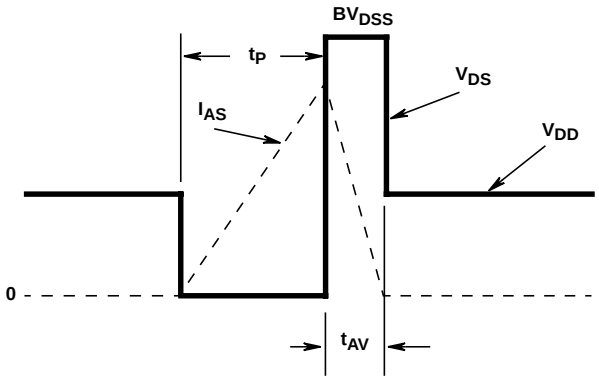


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

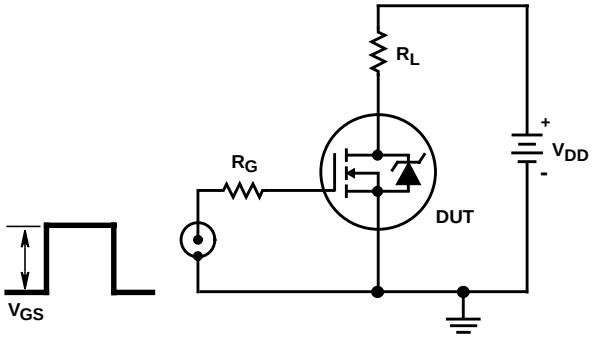


FIGURE 17. SWITCHING TIME TEST CIRCUIT

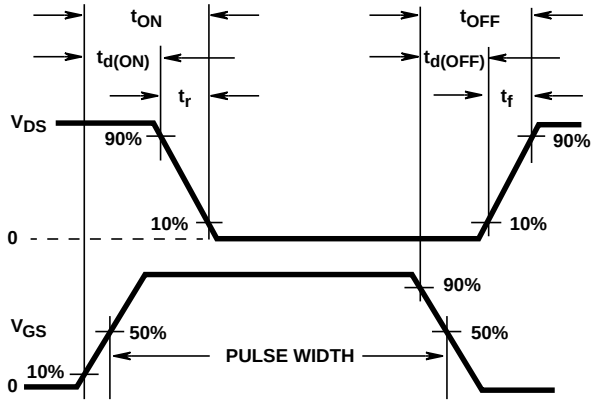


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

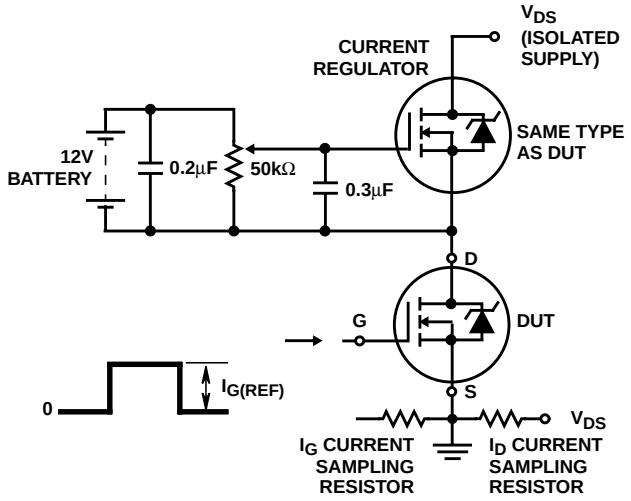


FIGURE 19. GATE CHARGE TEST CIRCUIT

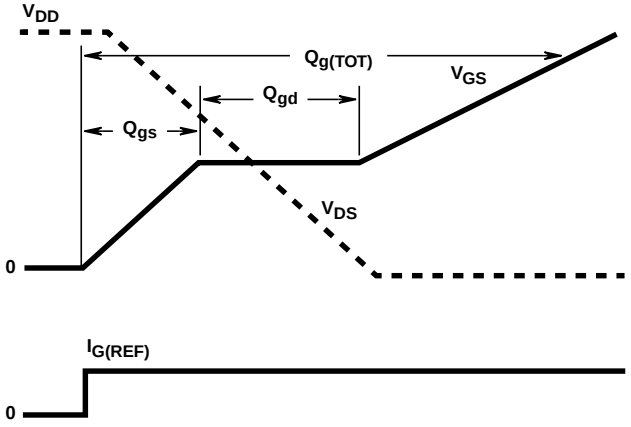


FIGURE 20. GATE CHARGE WAVEFORM